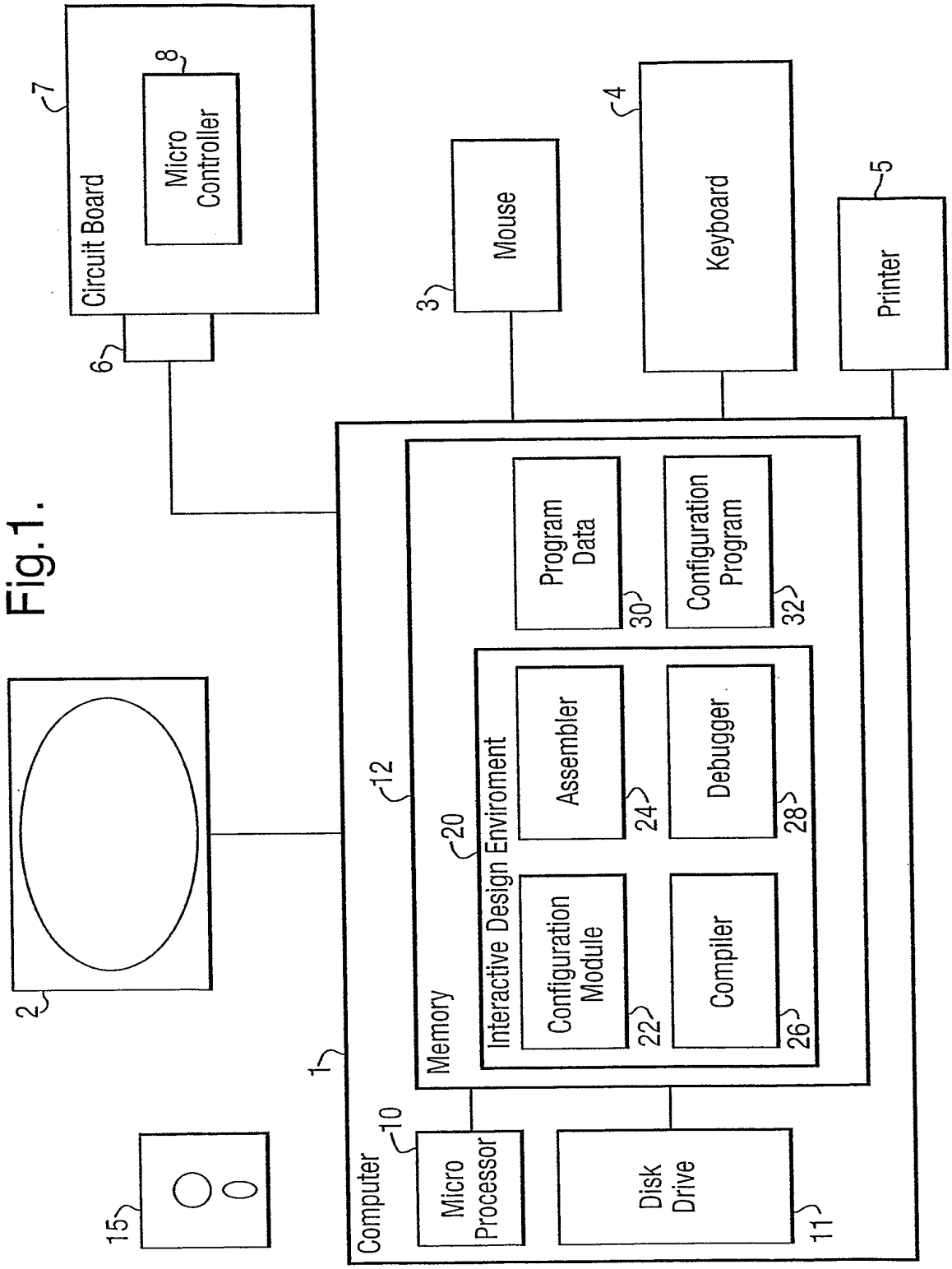

Circuit Board
Micro Controller
8
7
6
Mouse
3
Keyboard
4
Printer
5
2
1
Computer
Micro Processor
10
Disk Drive
11
15
Memory
12
Interactive Design Enviroment
20
Configuration Module
22
Assembler
24
Compiler
26
Debugger
28
Program Data
30
Configuration Program
32

Fig.1.

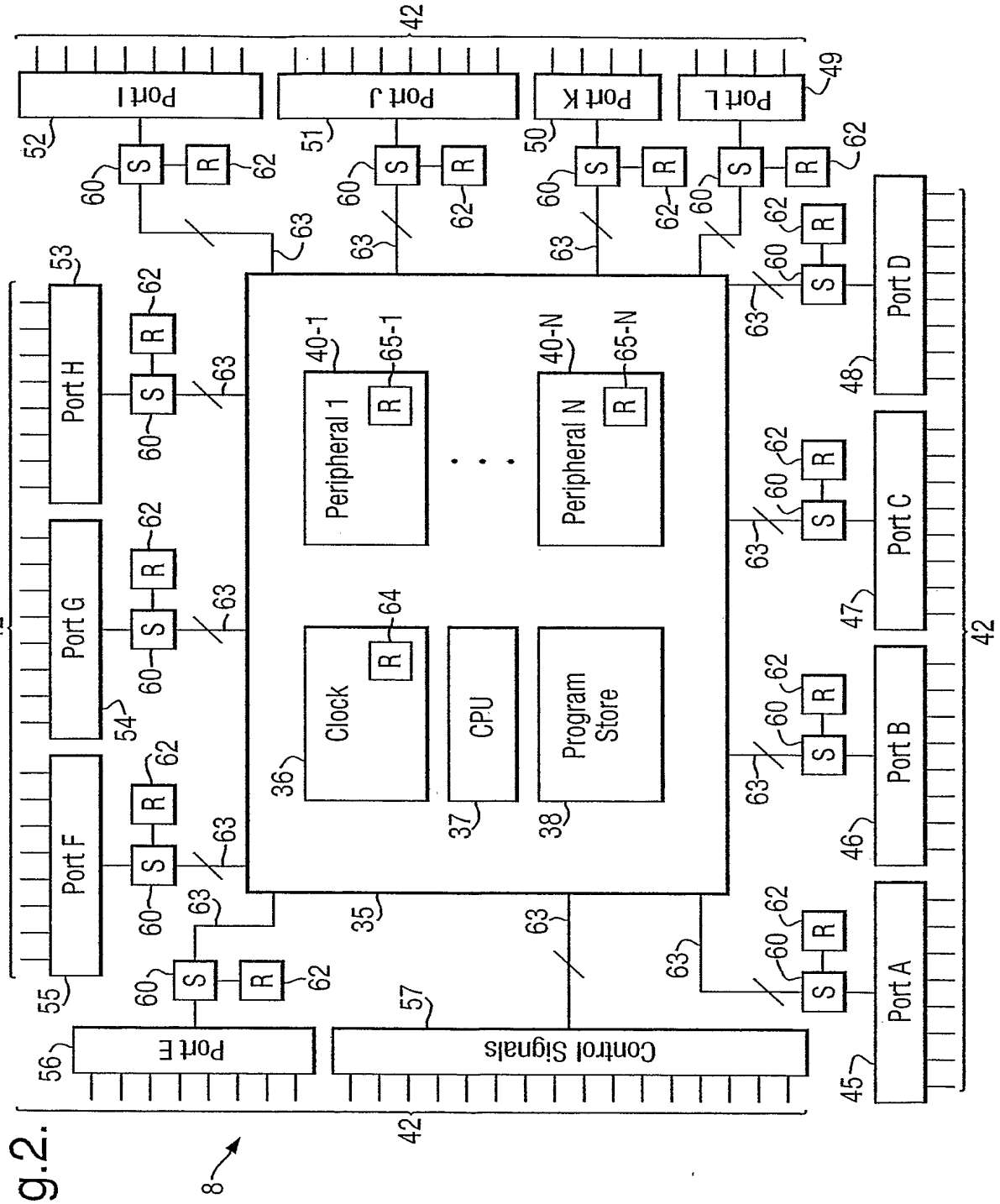

Port I
Port J
Port K
Port L
Port H
Port G
Port F
Port E
Port D
Port C
Port B
Port A
Control Signals
Peripheral 1
Peripheral N
Clock
CPU
Program Store
S
R
42
49
52
51
50
53
54
55
56
48
47
46
45
57
40-1
40-N
65-1
65-N
64
36
37
38
35
60
62
63

Fig.2.

Fig.3.

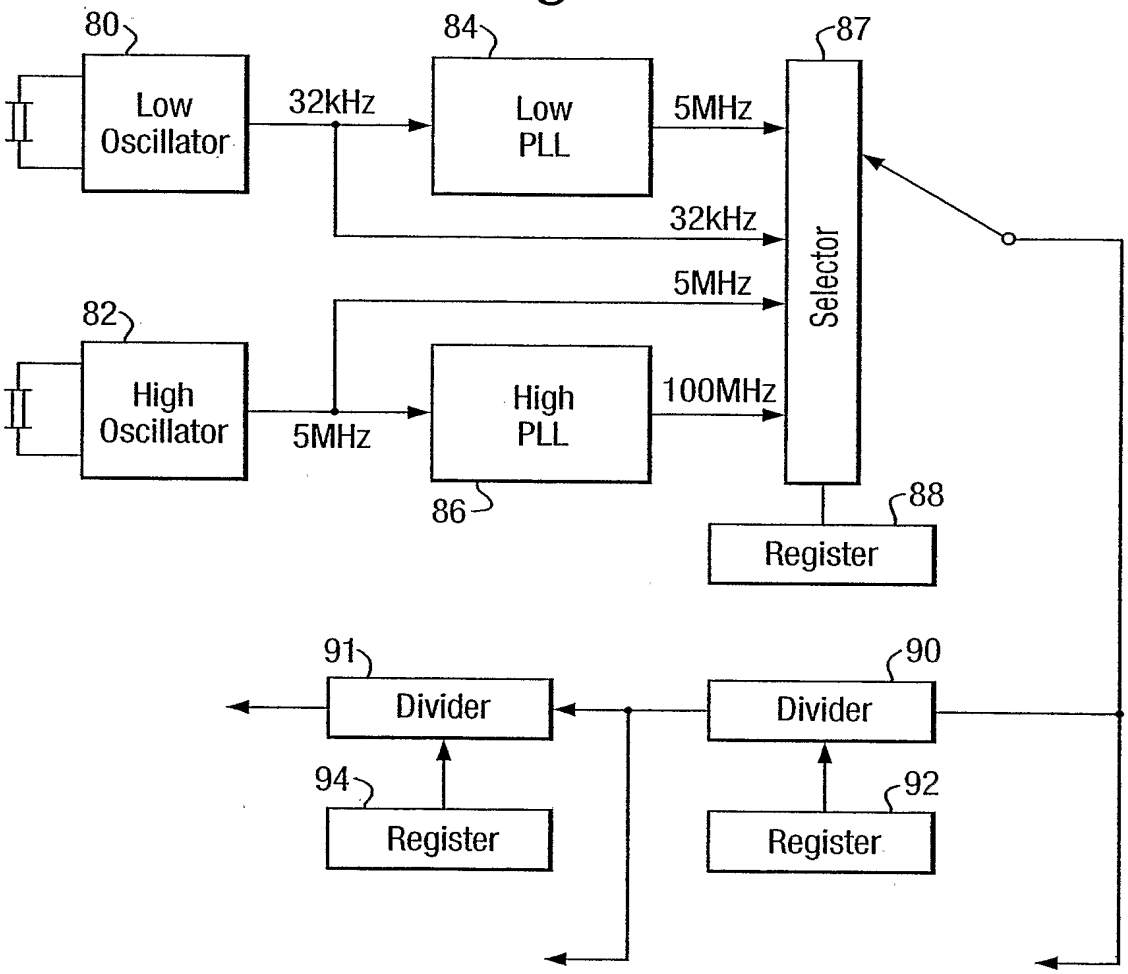

80
Low Oscillator
32kHz
84
Low PLL
5MHz
87
Selector
32kHz
5MHz
82
High Oscillator
5MHz
High PLL
100MHz
86
88
Register
91
Divider
90
Divider
94
Register
92
Register

Fig.4.

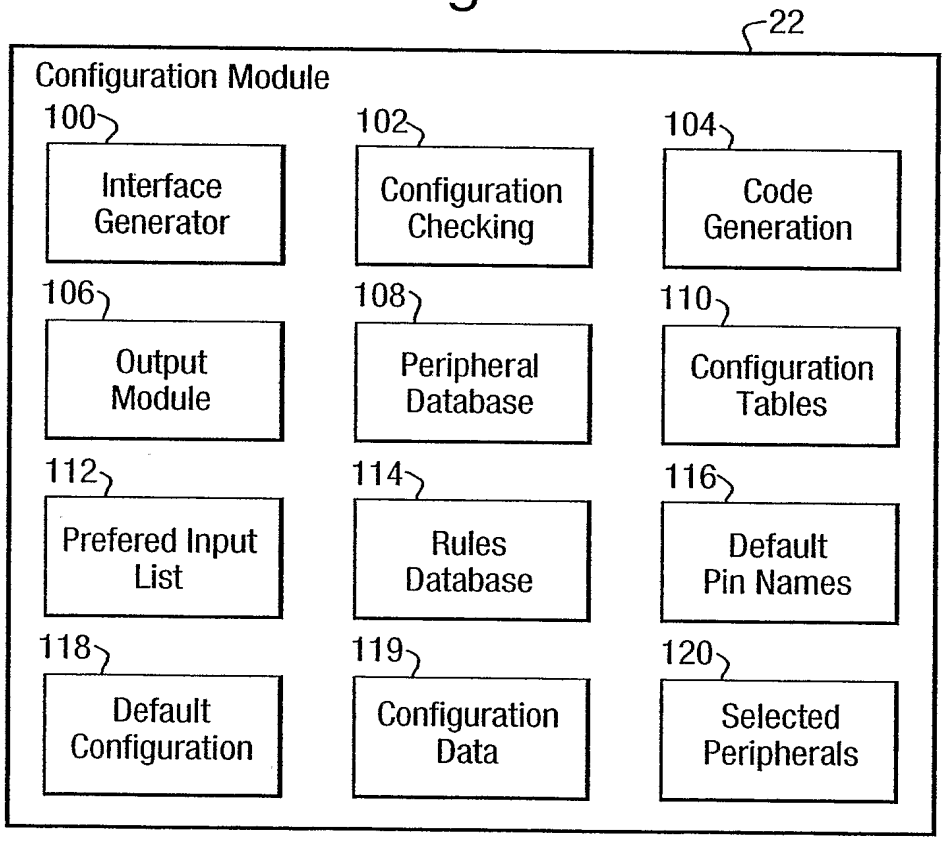

22
Configuration Module
100
Interface Generator
102
Configuration Checking
104
Code Generation
106
Output Module
108
Peripheral Database
110
Configuration Tables
112
Prefered Input List
114
Rules Database
116
Default Pin Names
118
Default Configuration
119
Configuration Data
120
Selected Peripherals

Fig.5.

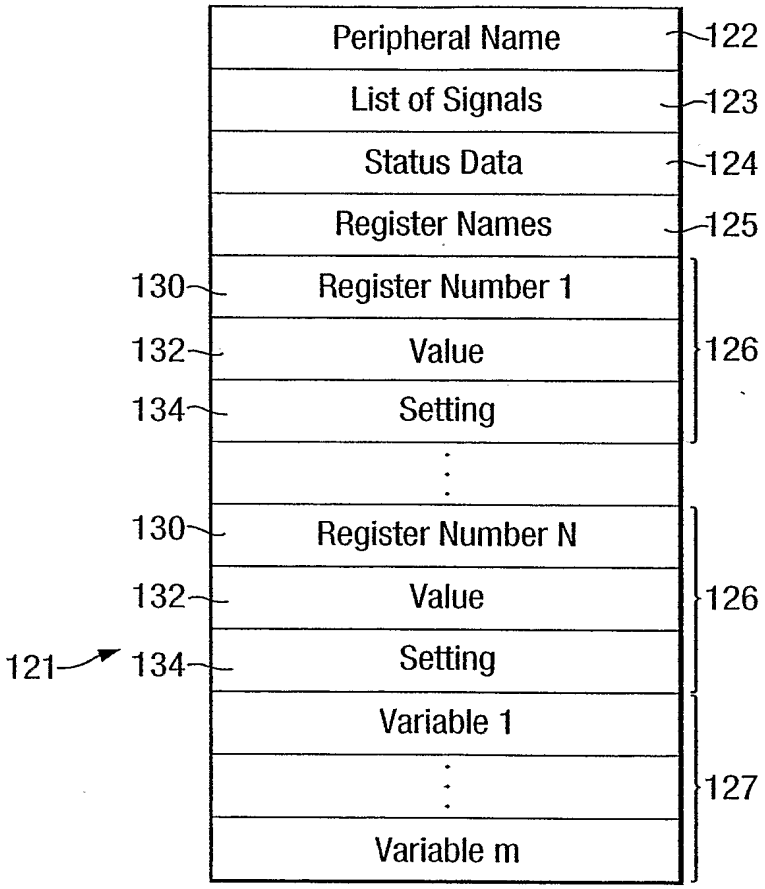

Peripheral Name
122
List of Signals
123
Status Data
124
Register Names
125
130
Register Number 1
132
Value
134
Setting
126
130
Register Number N
132
Value
121
134
Setting
126
Variable 1
Variable m
127

Fig.6.

135 136

Pin Number	Channel 0	Channel 1	Channel 2	Channel 3
62	WAKEUP	UARTB_RX	PWM1	WAKEUP
64	STREAM_ACK	UARTB_TX	PWM2	GPIO25
65	STREAM_STS	GPIO21	UARTB_RX	GPIO27
66	STREAM_REQ	GPIO22	UARTB_TX	GPIO12

Fig.7.

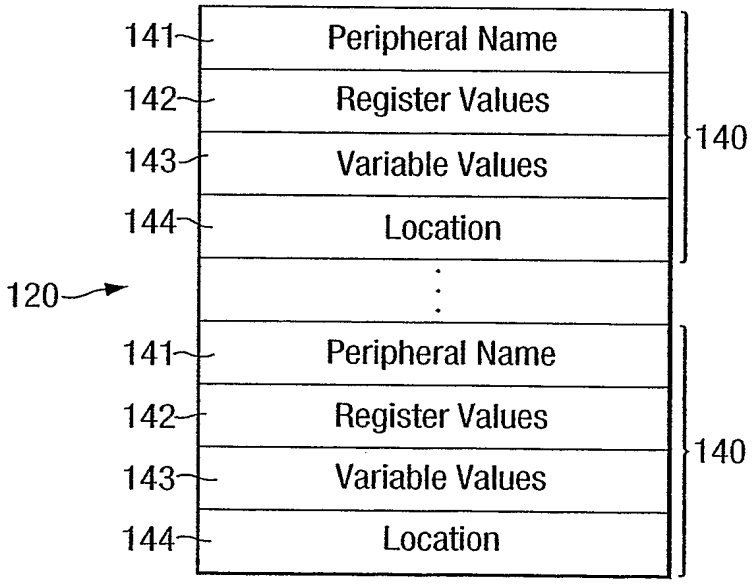
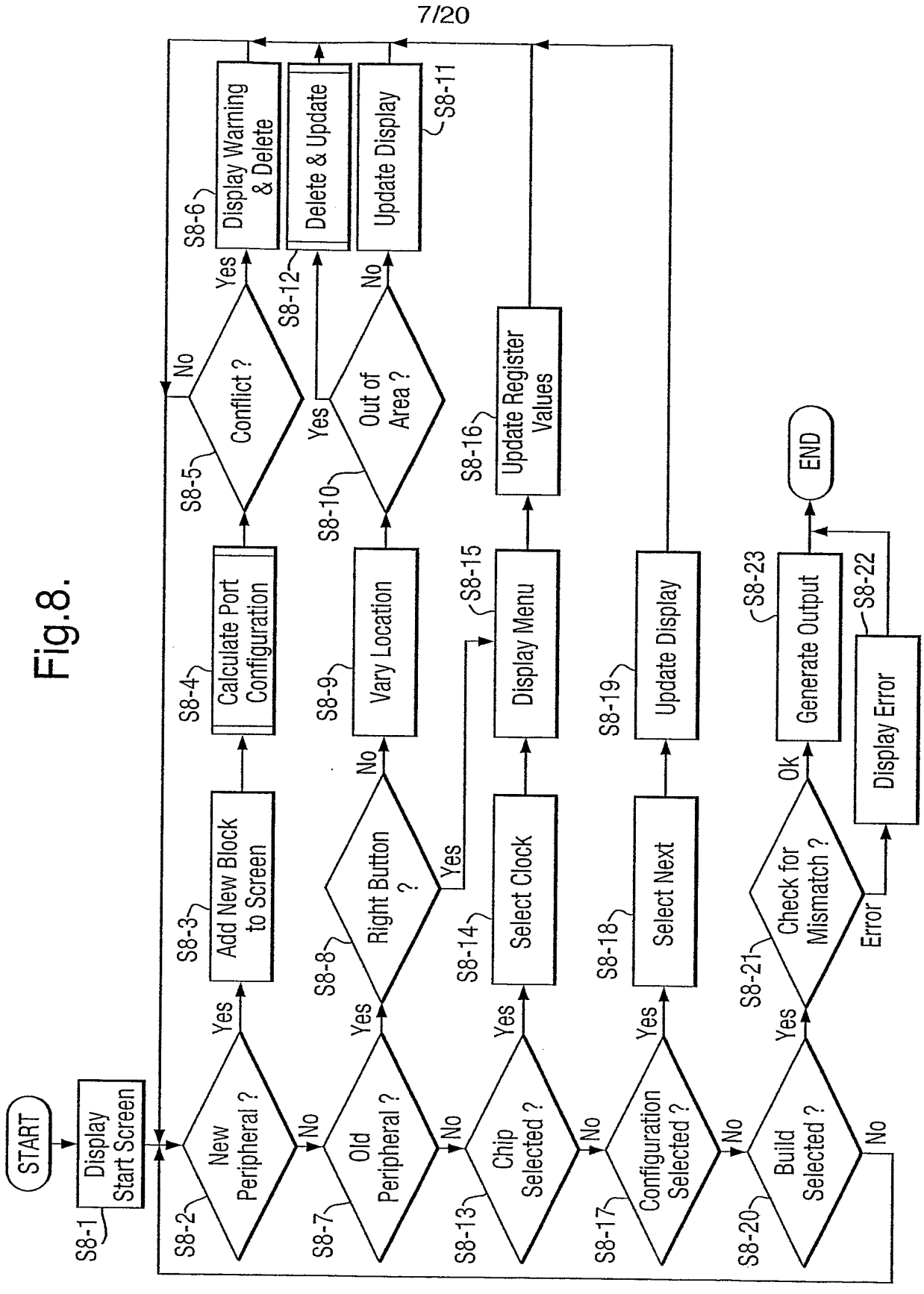


Fig.8.


START
Display Start Screen
S8-1
New Peripheral ?
S8-2
Yes
No
Add New Block to Screen
S8-3
Calculate Port Configuration
S8-4
Conflict ?
S8-5
Yes
No
Display Warning & Delete
S8-6
Old Peripheral ?
S8-7
Yes
No
Right Button ?
S8-8
No
Yes
Vary Location
S8-9
Out of Area ?
S8-10
Yes
No
Delete & Update
S8-12
Update Display
S8-11
Chip Selected ?
S8-13
Yes
No
Select Clock
S8-14
Display Menu
S8-15
Update Register Values
S8-16
Configuration Selected ?
S8-17
Yes
No
Select Next
S8-18
Update Display
S8-19
Build Selected ?
S8-20
Yes
No
Check for Mismatch ?
S8-21
Ok
Error
Generate Output
S8-23
Display Error
S8-22
END

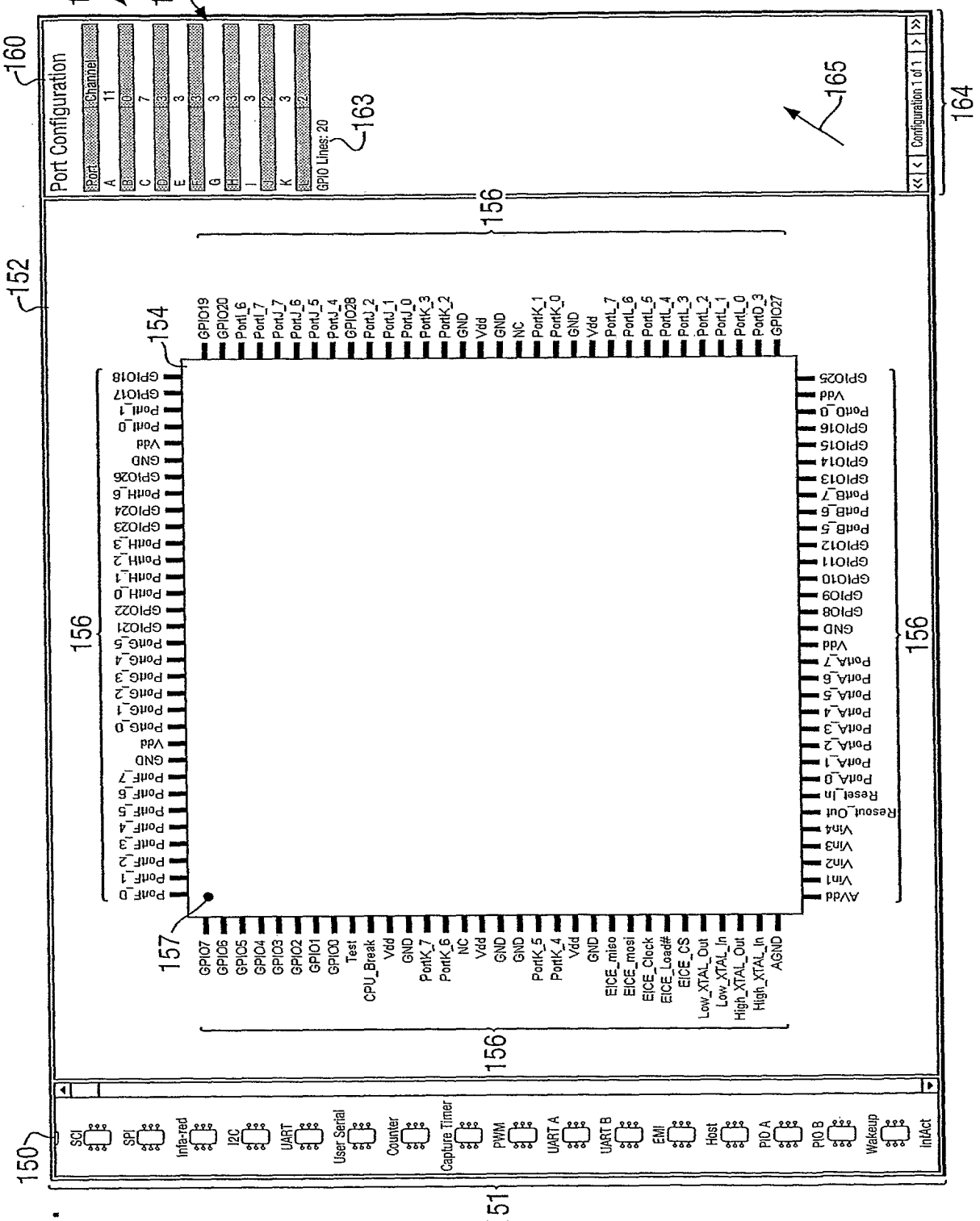
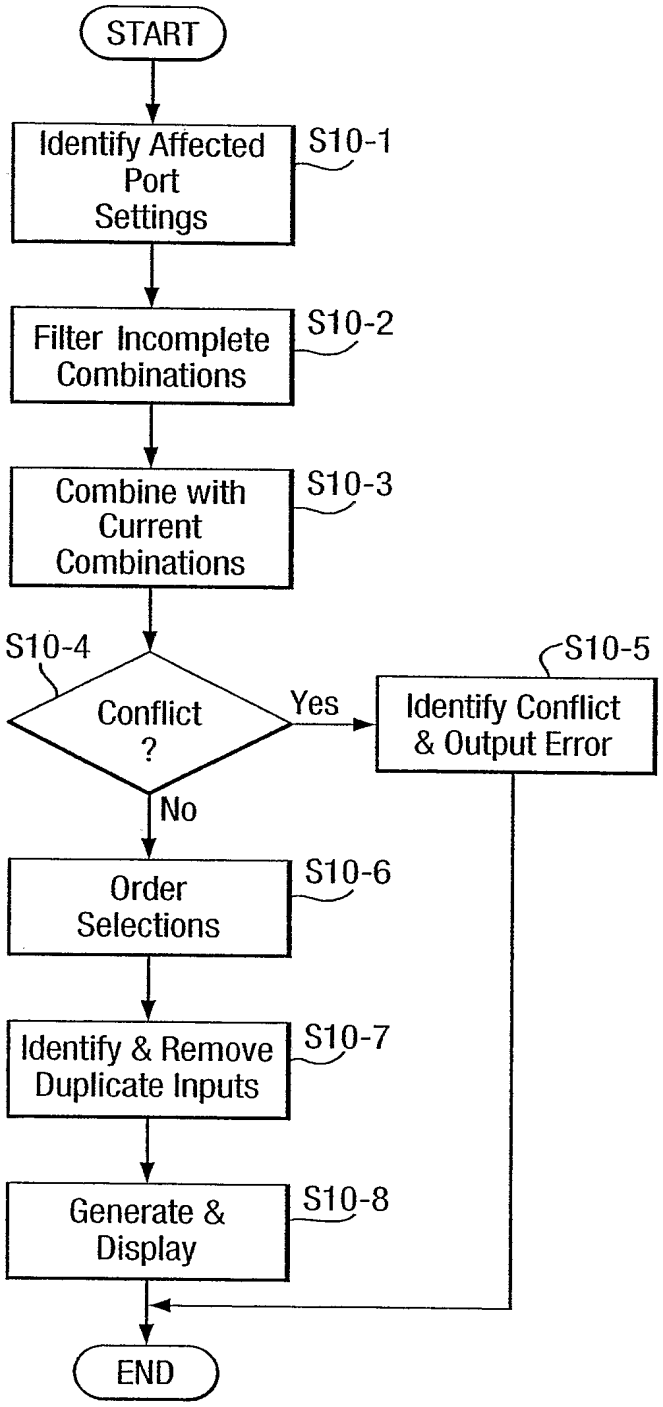

Port Configuration
Port
Channel
A 11
B 10
C 7
D 3
E 3
F 3
G 3
H 3
I 3
J 2
K 3
L 2
GPIO Lines: 20
Configuration 1 of 1
GPIO19 GPIO20 PortI_6 PortI_7 PortJ_7 PortJ_6 PortJ_5 PortJ_4 GPIO28 PortJ_2 PortJ_1 PortJ_0 PortK_3 PortK_2 GND Vdd GND NC PortK_1 PortK_0 GND Vdd PortL_7 PortL_6 PortL_6 PortL_4 PortL_3 PortL_2 PortL_1 PortL_0 PortD_3 GPIO27
GPIO25 Vdd PortD_0 GPIO16 GPIO15 GPIO14 GPIO13 PortB_7 PortB_6 PortB_5 GPIO12 GPIO11 GPIO10 GPIO9 GPIO8 GND Vdd PortA_7 PortA_6 PortA_5 PortA_4 PortA_3 PortA_2 PortA_1 PortA_0 Reset_In Resout_Out Vin4 Vin3 Vin2 Vin1 AVdd
PortF_0 PortF_1 PortF_2 PortF_3 PortF_4 PortF_5 PortF_6 PortF_7 GND Vdd PortG_0 PortG_1 PortG_2 PortG_3 PortG_4 PortG_5 GPIO21 GPIO22 PortH_0 PortH_1 PortH_2 PortH_3 GPIO23 GPIO24 PortH_6 GPIO26 GND Vdd PortI_0 PortI_1 GPIO17 GPIO18
GPIO7 GPIO6 GPIO5 GPIO4 GPIO3 GPIO2 GPIO1 GPIO0 Test CPU_Break Vdd GND PortK_7 PortK_6 NC Vdd GND GND PortK_5 PortK_4 Vdd GND EICE_miso EICE_mosi EICE_Clock EICE_Load# EICE_CS Low_XTAL_Out Low_XTAL_In High_XTAL_Out High_XTAL_In AGND
SCI SPI Infra-red I2C UART User Serial Counter Capture Timer PWM UART A UART B EMI Host PIO A PIO B Wakeup IntAct
150
151
152
154
156
157
160
162
163
164
165

Fig.9.

Fig.10.


START
Identify Affected Port Settings
S10-1
Filter Incomplete Combinations
S10-2
Combine with Current Combinations
S10-3
S10-4
Conflict ?
Yes
S10-5
Identify Conflict & Output Error
No
Order Selections
S10-6
Identify & Remove Duplicate Inputs
S10-7
Generate & Display
S10-8
END

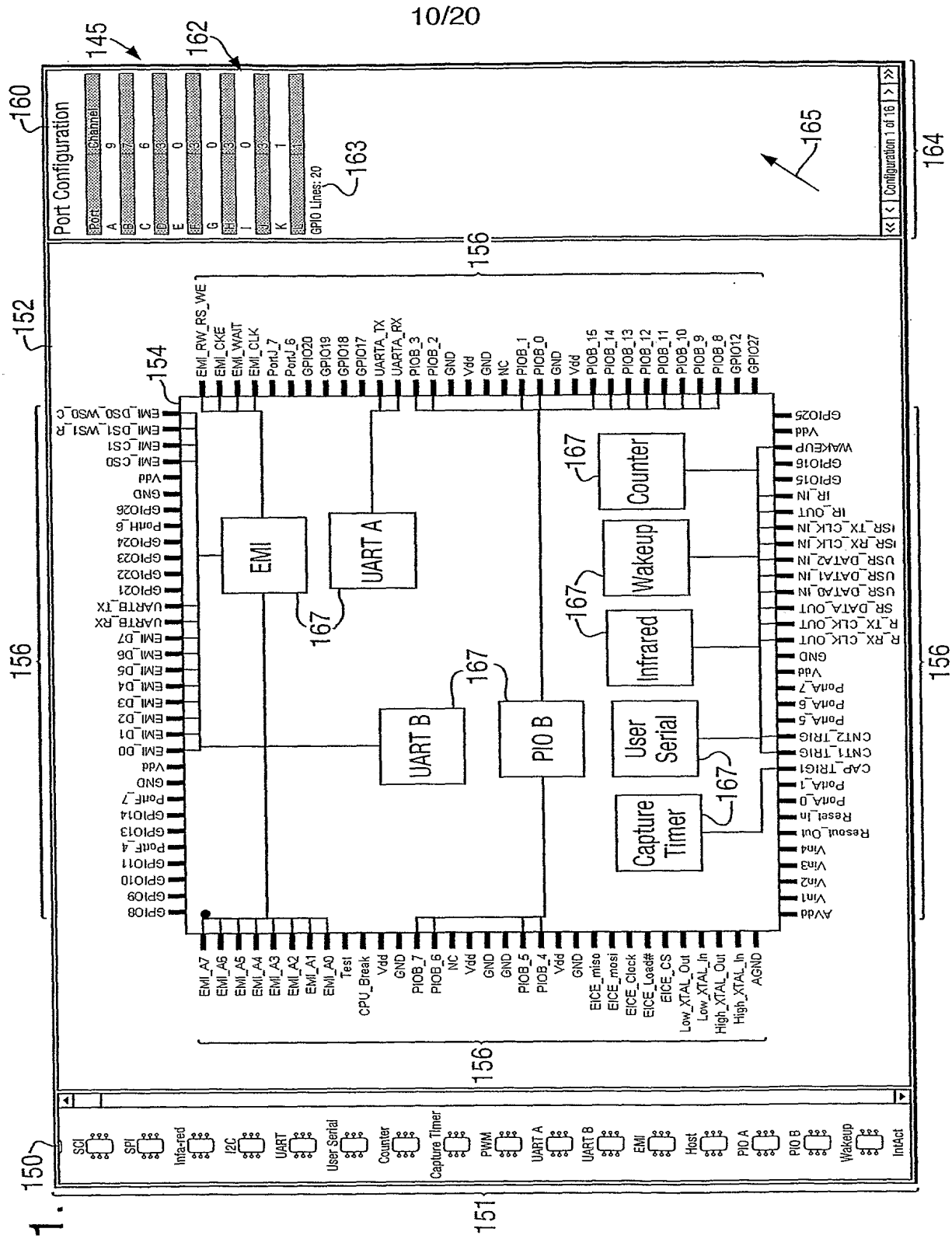

Port Configuration
Port
Channel
GPIO Lines: 20
Configuration 1 of 16
EMI
UART A
UART B
PIO B
Counter
Wakeup
Infrared
User Serial
Capture Timer
SCI
SPI
Infa-red
I2C
UART
User Serial
Counter
Capture Timer
PWM
UART A
UART B
EMI
Host
PIO A
PIO B
Wakeup
IntAct

Fig.11.

Fig.12.

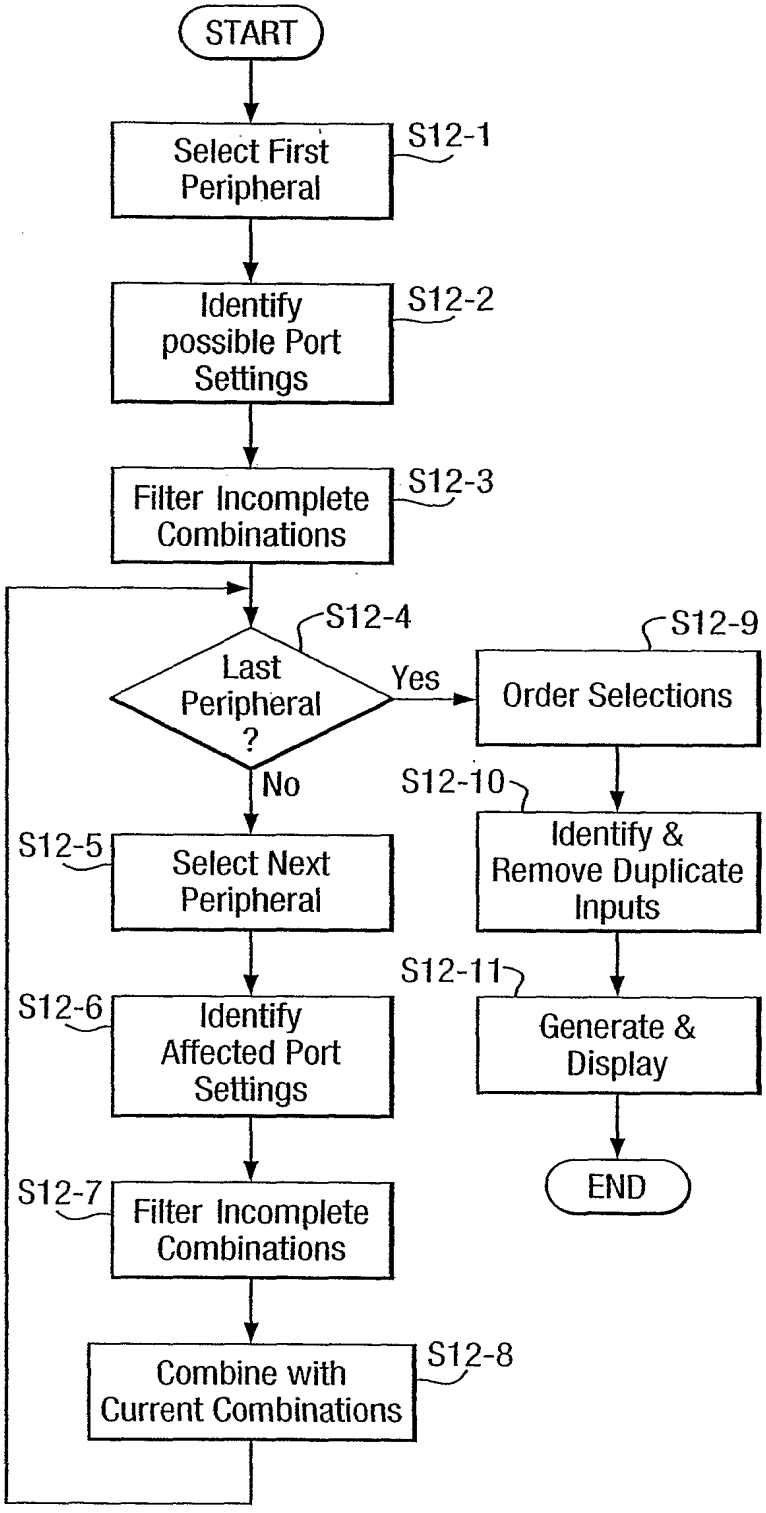

START
Select First Peripheral
S12-1
Identify possible Port Settings
S12-2
Filter Incomplete Combinations
S12-3
S12-4
Last Peripheral ?
Yes
S12-9
Order Selections
No
S12-10
Identify & Remove Duplicate Inputs
S12-5
Select Next Peripheral
S12-11
S12-6
Identify Affected Port Settings
Generate & Display
END
S12-7
Filter Incomplete Combinations
S12-8
Combine with Current Combinations

Fig.13.

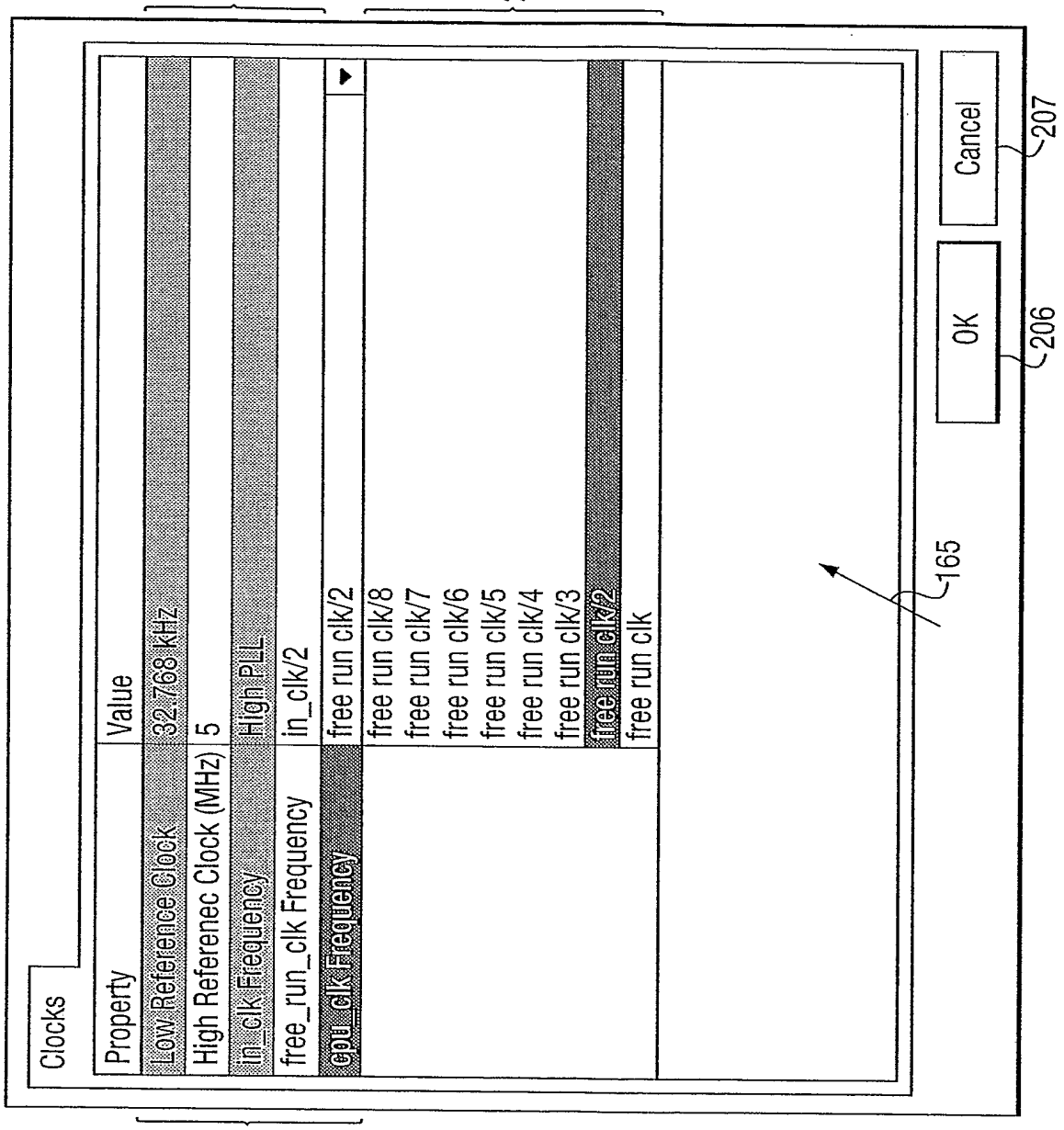

Clocks
Property
Value
Low Reference Clock
32.768 kHz
High Referenec Clock (MHz)
5
in_clk Frequency
High PLL
free_run_clk Frequency
in_clk/2
cpu_clk Frequency
free run clk/2
free run clk/8
free run clk/7
free run clk/6
free run clk/5
free run clk/4
free run clk/3
free run clk/2
free run clk
200
202
204
165
OK
206
Cancel
207

Fig.14.

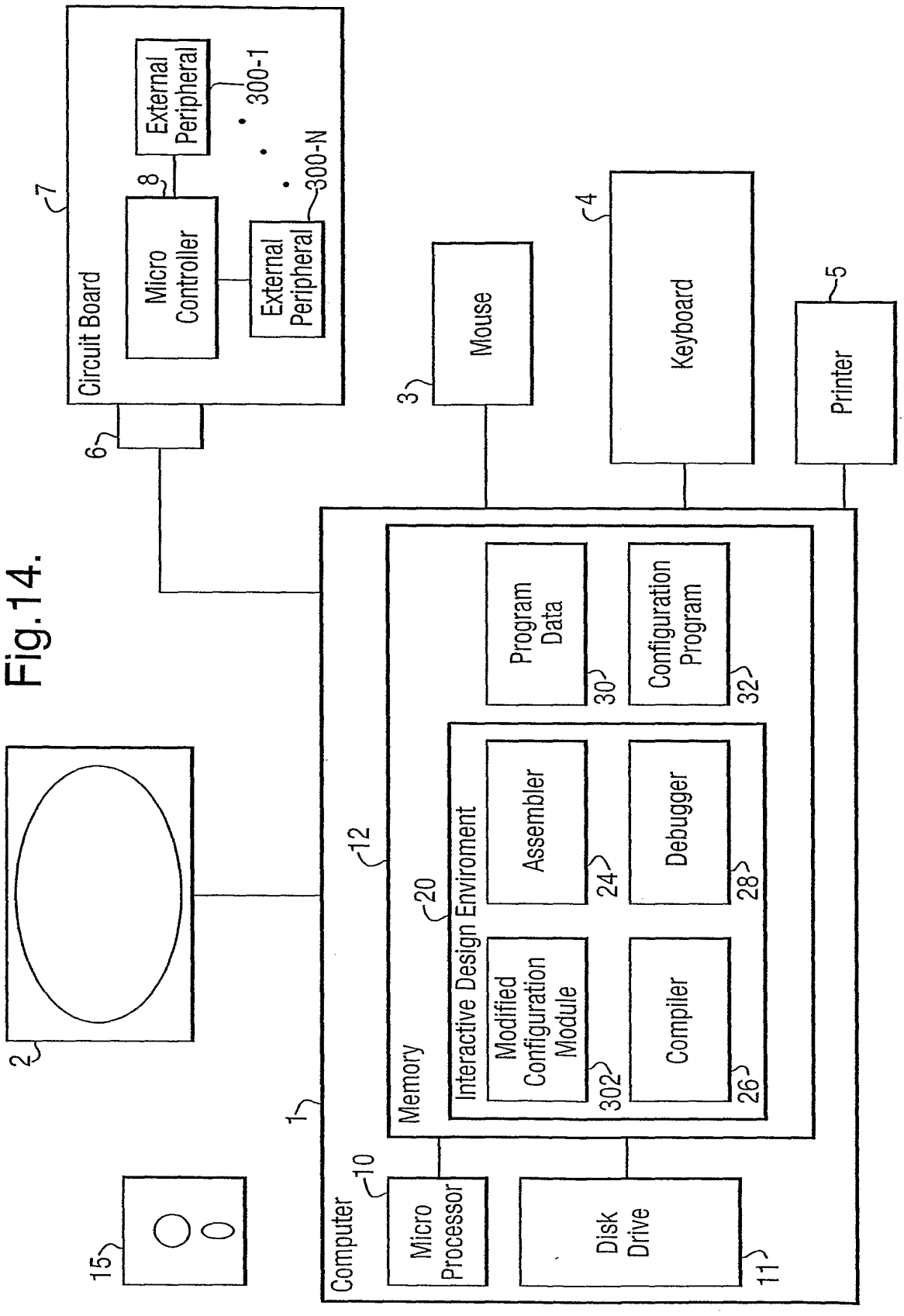

Circuit Board
7
Micro Controller
8
External Peripheral
300-1
300-N
External Peripheral
6
Mouse
3
Keyboard
4
Printer
5
2
Computer
1
Micro Processor
10
Disk Drive
11
15
Memory
12
Program Data
30
Configuration Program
32
Interactive Design Enviroment
20
Assembler
24
Debugger
28
Modified Configuration Module
302
Compiler
26

Fig.15.

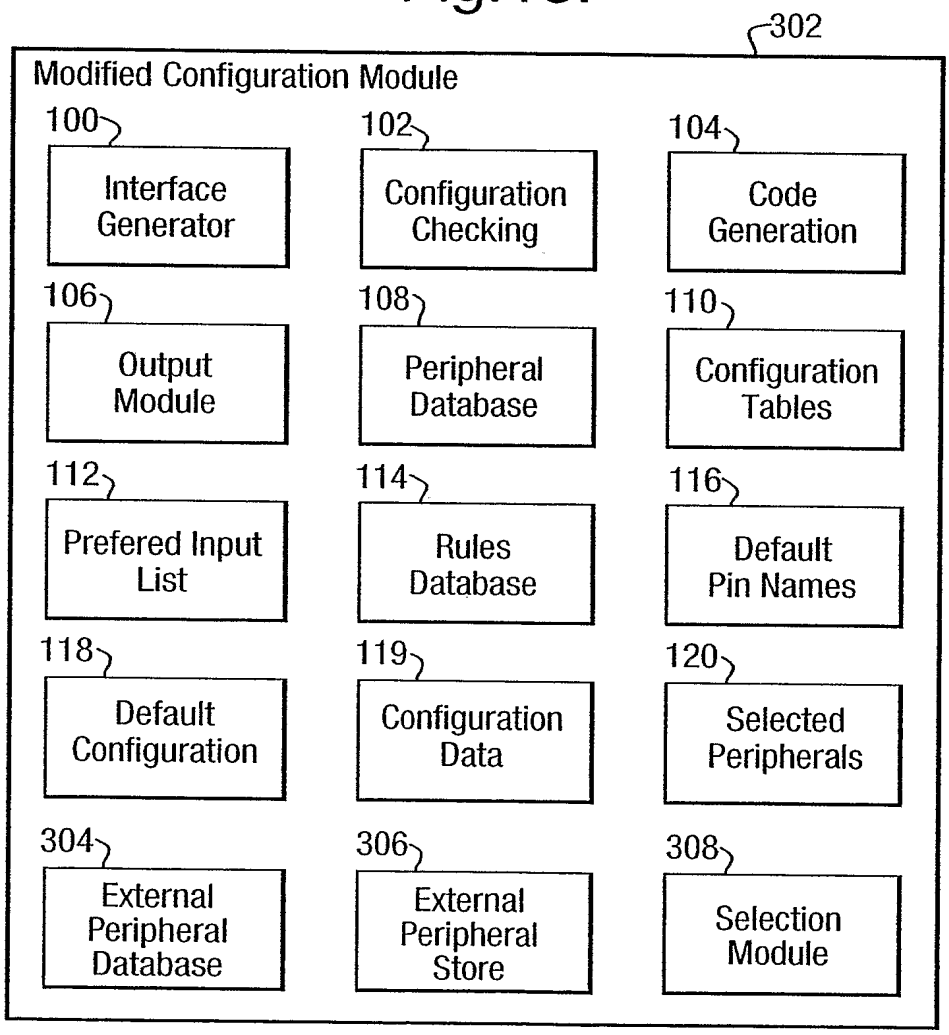

302
Modified Configuration Module
100
Interface Generator
102
Configuration Checking
104
Code Generation
106
Output Module
108
Peripheral Database
110
Configuration Tables
112
Prefered Input List
114
Rules Database
116
Default Pin Names
118
Default Configuration
119
Configuration Data
120
Selected Peripherals
304
External Peripheral Database
306
External Peripheral Store
308
Selection Module

Fig.16.

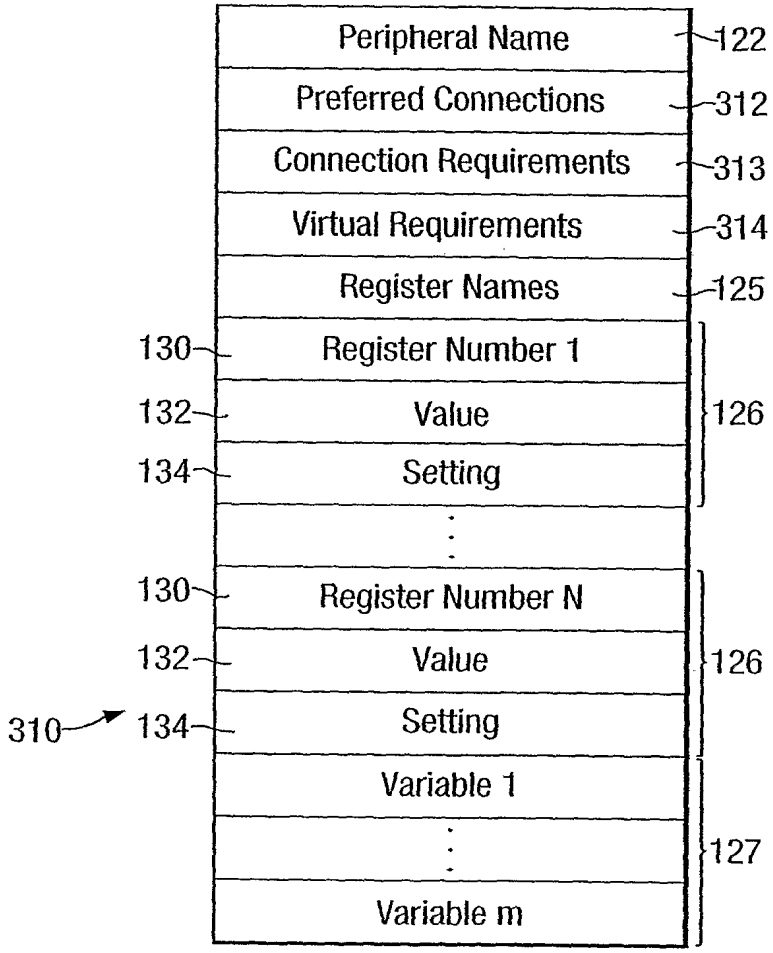
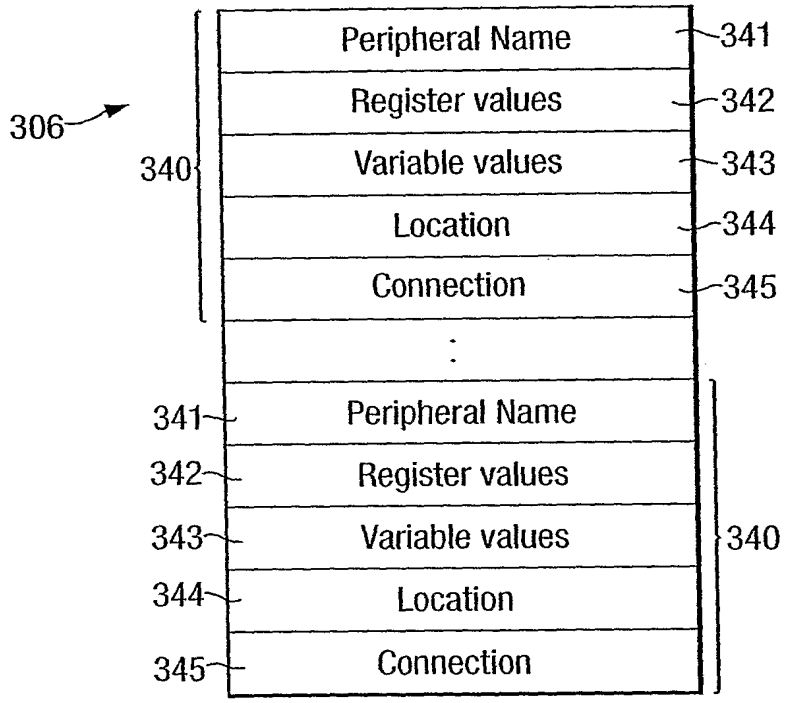

Peripheral Name
122
Preferred Connections
312
Connection Requirements
313
Virtual Requirements
314
Register Names
125
130
Register Number 1
132
Value
134
Setting
126
130
Register Number N
132
Value
310
134
Setting
126
Variable 1
127
Variable m

Fig.17.


306
340
Peripheral Name
341
Register values
342
Variable values
343
Location
344
Connection
345
341
Peripheral Name
342
Register values
343
Variable values
344
Location
345
Connection
340

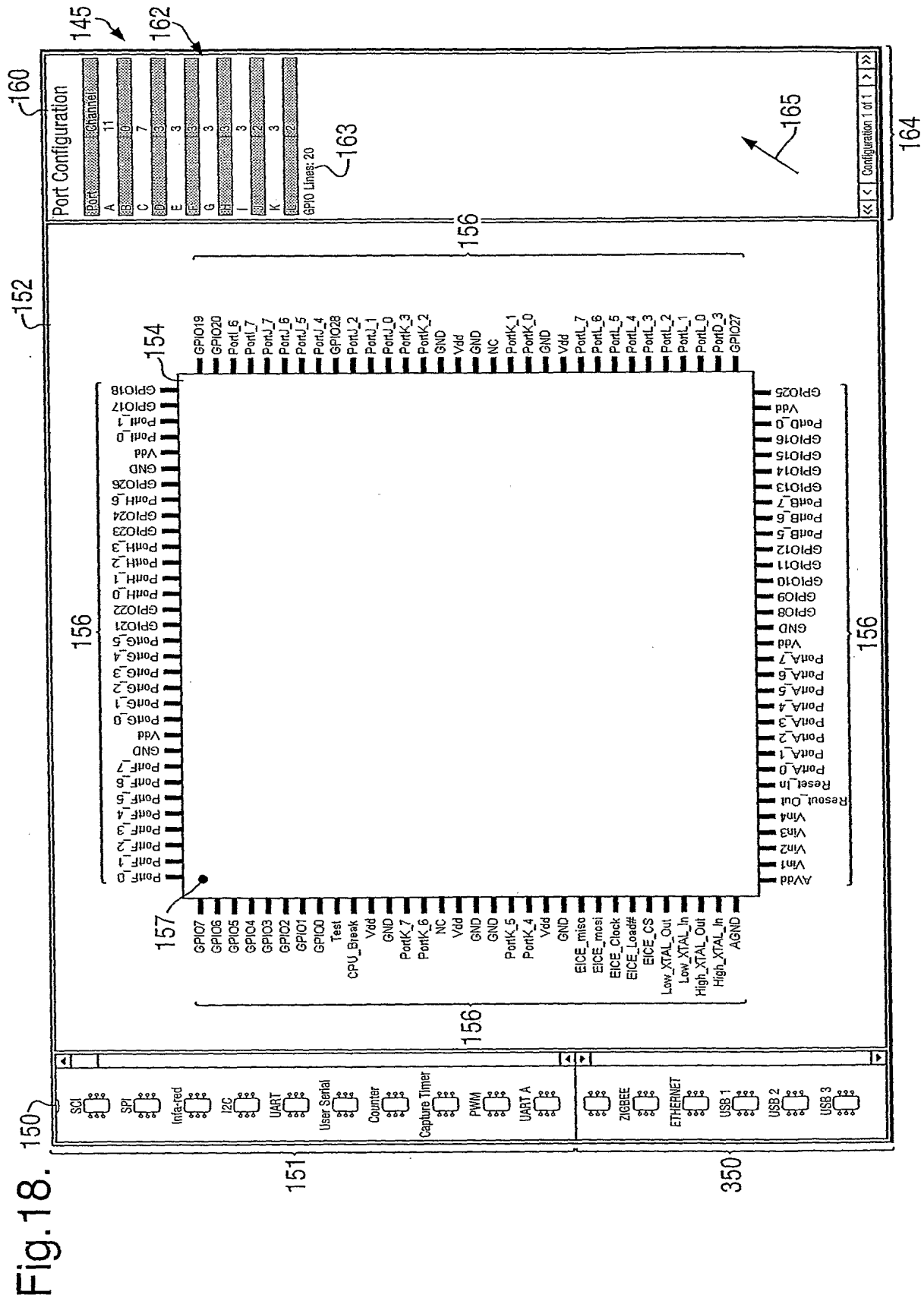
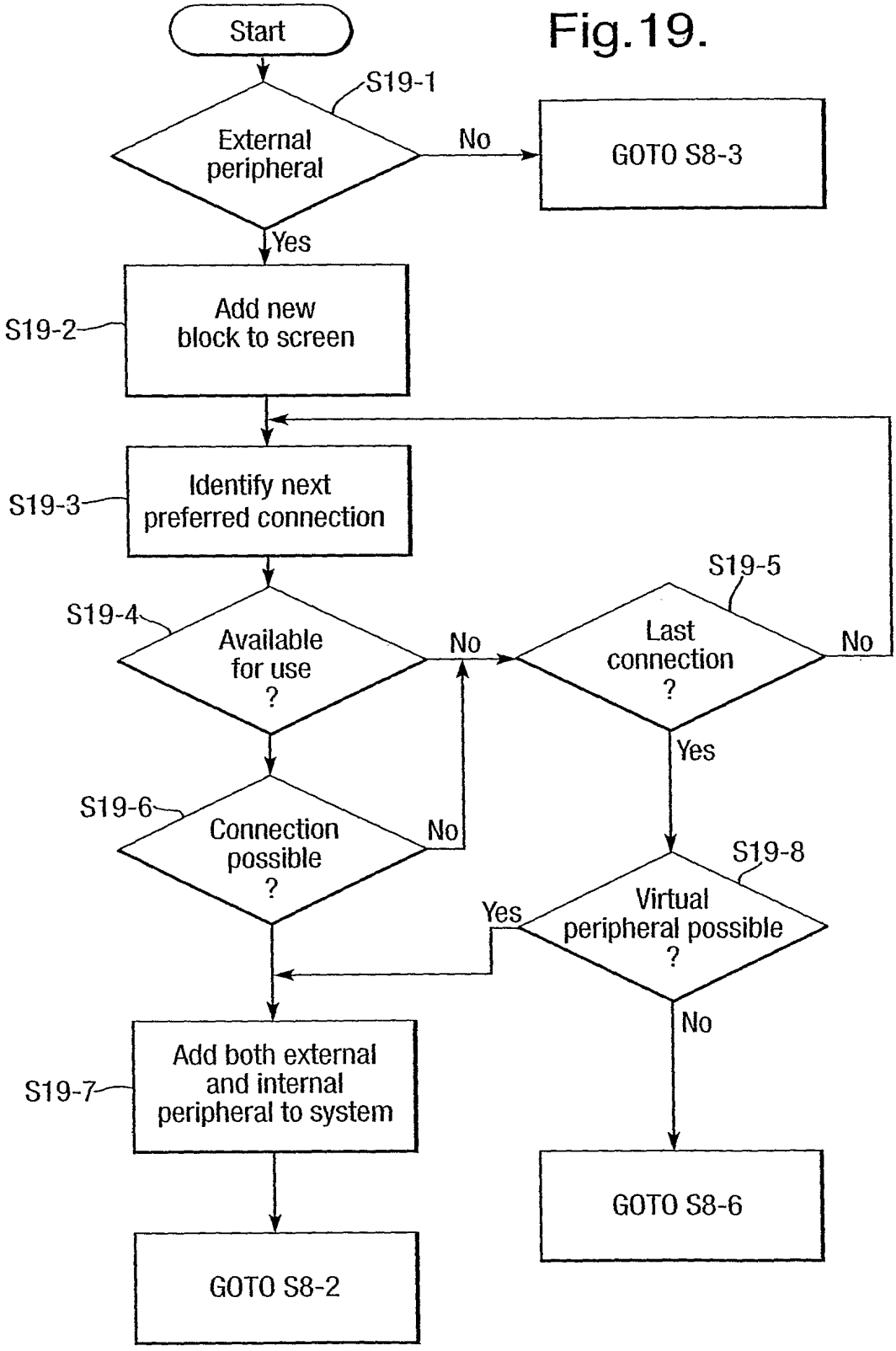

Port Configuration
Port
Channel
A 11
B 10
C 7
D 6
E 3
F 15
G 3
H 13
I 3
J 12
K 3
L 12
GPIO Lines: 20
Configuration 1 of 1
145
162
160
163
165
164
152
154
156
157
GPIO19 GPIO20 PortL_6 PortL_7 PortJ_7 PortJ_6 PortJ_5 PortJ_4 GPIO28 PortJ_2 PortJ_1 PortJ_0 PortK_3 PortK_2 GND Vdd GND NC PortK_1 PortK_0 GND Vdd PortL_7 PortL_6 PortL_5 PortL_4 PortL_3 PortL_2 PortL_1 PortL_0 PortD_3 GPIO27
GPIO18 GPIO17 PortI_1 PortI_0 Vdd GND GPIO26 PortH_6 GPIO24 GPIO23 PortH_3 PortH_2 PortH_1 PortH_0 GPIO22 GPIO21 PortG_5 PortG_4 PortG_3 PortG_2 PortG_1 PortG_0 Vdd GND PortF_7 PortF_6 PortF_5 PortF_4 PortF_3 PortF_2 PortF_1 PortF_0
GPIO25 Vdd PortD_0 GPIO16 GPIO15 GPIO14 GPIO13 PortB_7 PortB_6 PortB_5 GPIO12 GPIO11 GPIO10 GPIO9 GPIO8 GND Vdd PortA_7 PortA_6 PortA_5 PortA_4 PortA_3 PortA_2 PortA_1 PortA_0 Reset_In Resout_Out Vin4 Vin3 Vin2 Vin1 AVdd
GPIO7 GPIO6 GPIO5 GPIO4 GPIO3 GPIO2 GPIO1 GPIO0 Test CPU_Break Vdd GND PortK_7 PortK_6 NC Vdd GND GND PortK_5 PortK_4 Vdd GND EICE_miso EICE_mosi EICE_Clock EICE_Load# EICE_CS Low_XTAL_Out Low_XTAL_In High_XTAL_Out High_XTAL_In AGND
156
150
151
350
SCI SPI Infra-red I2C UART User Serial Counter Capture Timer PWM UART A
ZIGBEE ETHERNET USB 1 USB 2 USB 3

Fig.18.

Fig.19.


Start
S19-1
External peripheral
No
GOTO S8-3
Yes
S19-2
Add new block to screen
S19-3
Identify next preferred connection
S19-4
Available for use ?
No
S19-5
Last connection ?
No
Yes
S19-6
Connection possible ?
No
S19-8
Virtual peripheral possible ?
Yes
No
S19-7
Add both external and internal peripheral to system
GOTO S8-6
GOTO S8-2

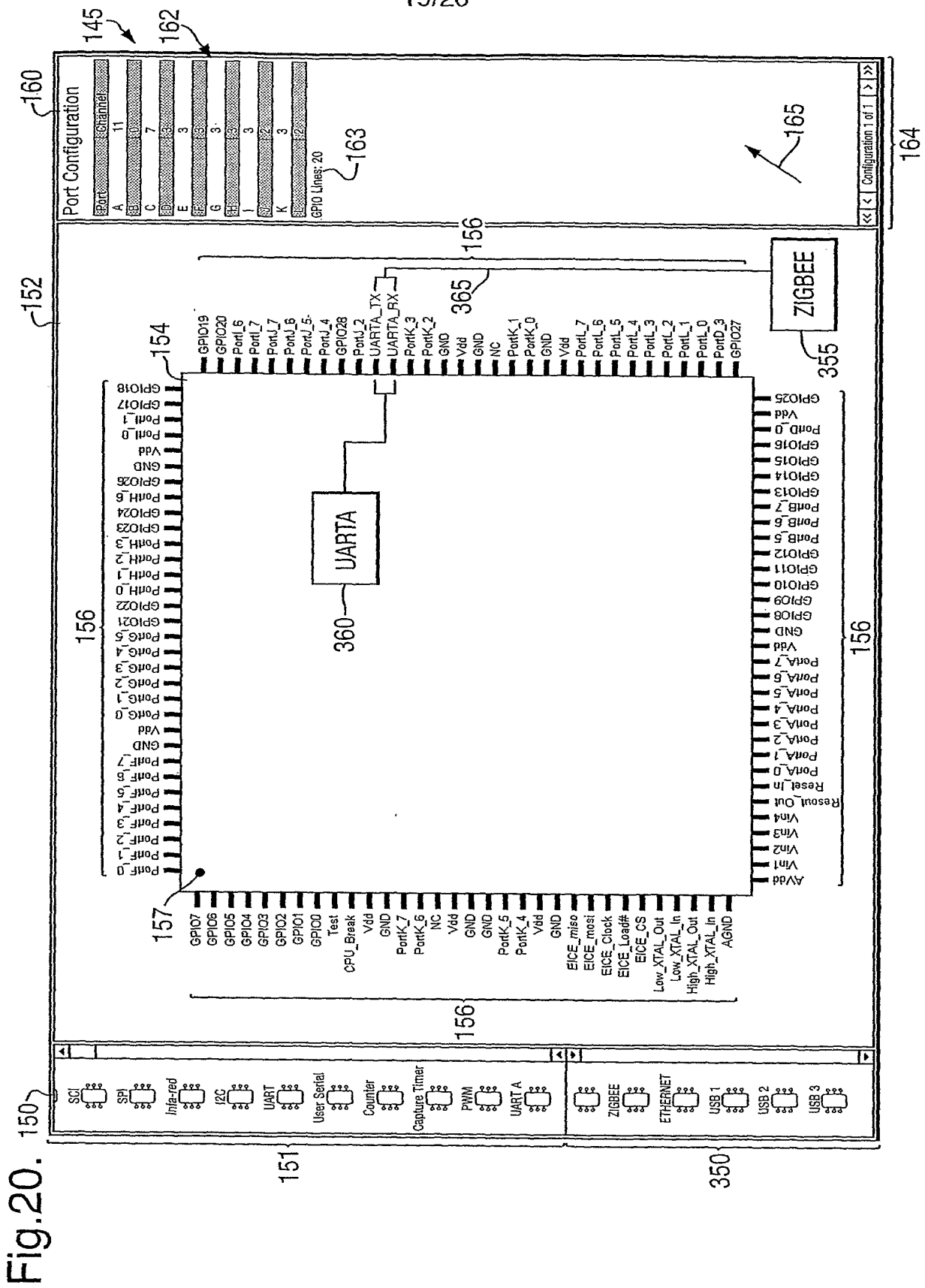

Port Configuration
Port
Channel
A 11
B 10
C 7
D 3
E 3
F 3
G 3
H 3
I 3
J 2
K 3
L 2
GPIO Lines: 20
Configuration 1 of 1
ZIGBEE
UARTA
UARTA_TX
UARTA_RX
SCI
SPI
Infra-red
I2C
UART
User Serial
Counter
Capture Timer
PWM
UART A
ZIGBEE
ETHERNET
USB 1
USB 2
USB 3
145
162
160
163
164
165
152
154
156
157
355
360
365
150
151
350

Fig.20.

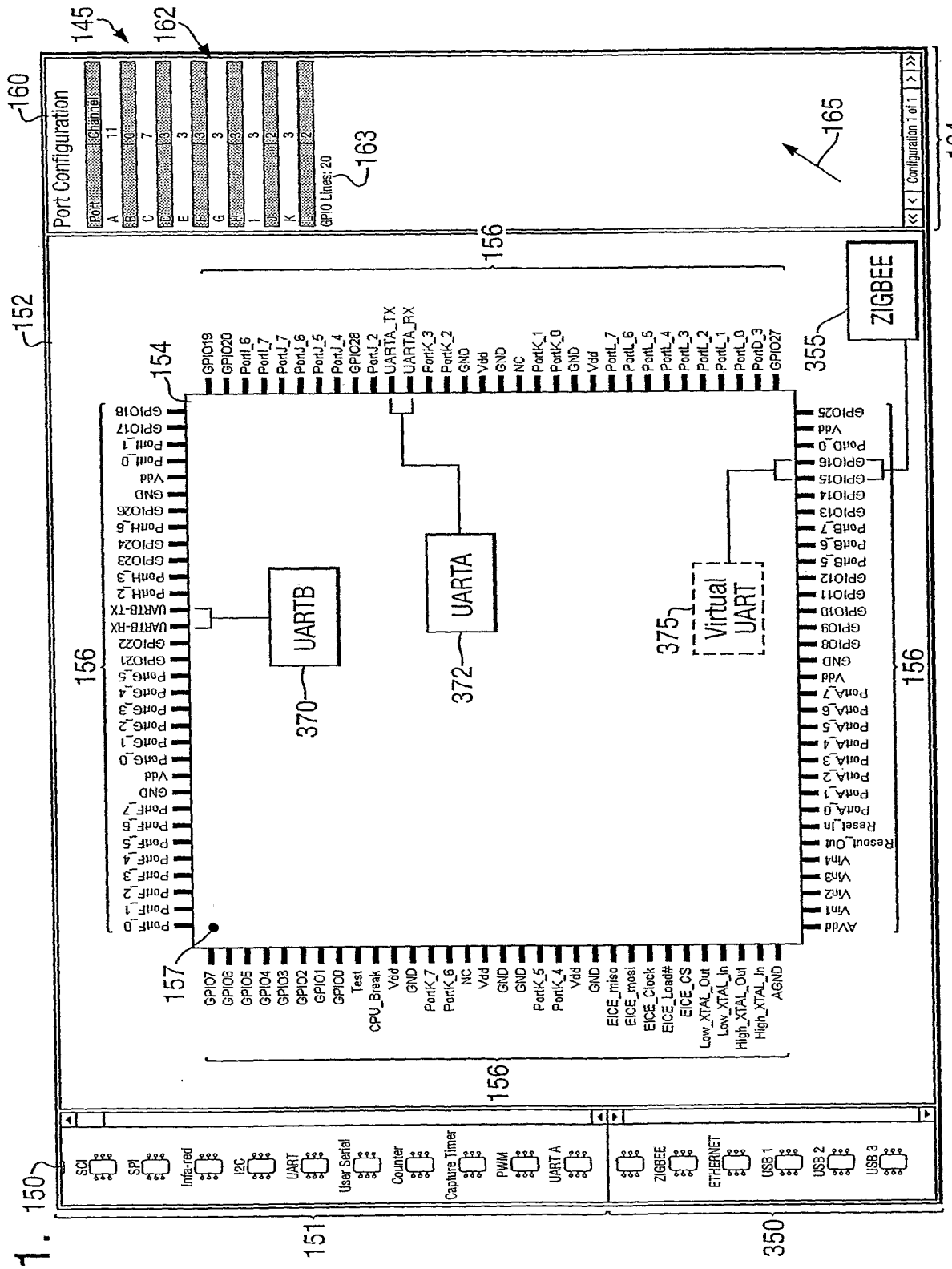

Port Configuration
Port
Channel
A
11
B
0
C
7
D
3
E
3
F
3
G
3
H
3
I
3
J
3
K
3
L
2
GPIO Lines: 20
Configuration 1 of 1
145
162
160
163
165
164
152
156
154
355
ZIGBEE
GPIO19
GPIO20
PortI_6
PortI_7
PortJ_7
PortJ_6
PortJ_5
PortJ_4
GPIO28
PortJ_2
UARTA_TX
UARTA_RX
PortK_3
PortK_2
GND
Vdd
GND
NC
PortK_1
PortK_0
GND
Vdd
PortL_7
PortL_6
PortL_5
PortL_4
PortL_3
PortL_2
PortL_1
PortL_0
PortD_3
GPIO27
GPIO18
GPIO17
PortI_1
PortI_0
Vdd
GND
PortH_6
GPIO26
GPIO24
GPIO23
PortH_3
PortH_2
UART-TX
UART-RX
GPIO22
GPIO21
PortG_5
PortG_4
PortG_3
PortG_2
PortG_1
PortG_0
Vdd
GND
PortF_7
PortF_6
PortF_5
PortF_4
PortF_3
PortF_2
PortF_1
PortF_0
156
370
UARTB
372
UARTA
375
Virtual
UART
GPIO25
Vdd
PortD_0
GPIO16
GPIO15
GPIO14
GPIO13
PortB_7
PortB_6
PortB_5
GPIO12
GPIO11
GPIO10
GPIO9
GPIO8
GND
Vdd
PortA_7
PortA_6
PortA_5
PortA_4
PortA_3
PortA_2
PortA_1
PortA_0
Reset_In
Resout_Out
Vin4
Vin3
Vin2
Vin1
AVdd
157
GPIO7
GPIO6
GPIO5
GPIO4
GPIO3
GPIO2
GPIO1
GPIO0
Test
CPU_Break
Vdd
GND
PortK_7
PortK_6
NC
Vdd
GND
GND
PortK_5
PortK_4
Vdd
GND
EICE_miso
EICE_mosi
EICE_Clock
EICE_Load#
EICE_CS
Low_XTAL_Out
Low_XTAL_In
High_XTAL_Out
High_XTAL_In
AGND
150
151
350
SCI
SPI
Infra-red
I2C
UART
User Serial
Counter
Capture Timer
PWM
UART A
ZIGBEE
ETHERNET
USB 1
USB 2
USB 3

Fig.21.